The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 46

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DONALD M. BARTLETT

Appeal No. 1999-1855
Application 08/738,916[1]

ON BRIEF

Before KRASS, BARRETT, and LALL, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

[1] Application for patent filed October 28, 1996, entitled "Negative Voltage Generator For Use With N-Well CMOS Processes," which is a continuation of Application 08/534,088, filed September 26, 1995, now abandoned, which is a continuation of Application 08/193,833, filed February 9, 1994, now abandoned.

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 8-10, 21, and 23. Claims 1-3, 7, 11-18, 20, and 22 have been canceled. Claims 4-6 and 19 are allowed.

We affirm-in-part.

BACKGROUND

The disclosed invention is directed to a voltage generator that is capable of generating negative voltage pulses using standard CMOS transistor switches that are formed directly in a p-type substrate or in n-wells that are formed in the p-type substrate (n-well CMOS process), as opposed to in an n-type substrate or p-wells in the n-type substrate (p-well CMOS process).

Claim 8 is reproduced below.

> 8. A low-voltage, semiconductor drive circuit comprising:
>
> a p-channel drive transistor having a source connected to a positive voltage source and a drain providing a drive output; and
>
> a voltage generator switchably providing a negative voltage to a gate of said p-channel transistor;
>
> wherein said voltage generator is fabricated using p-channel enhancement mode transistors formed in n-type wells in a grounded p-type substrate and n-channel

enhancement mode transistors formed in said grounded p-type substrate.

The Examiner relies on the admitted prior art (APA) in figure 3 and the specification at page 3.

The pending rejections are:

Claims 8-10 and 23 stand rejected under 35 U.S.C. § 112, first paragraph, for lack of an enabling disclosure.

Claims 8-10, 21, and 23 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the APA in figure 3 of the specification.[2]

We refer to the final rejection (Paper No. 30) and the examiner's answer (Paper No. 41) (pages referred to as "EA__") for a statement of the Examiner's position, and to the appeal brief (Paper No. 38) (pages referred to as "Br__") and the reply brief (Paper No. 42) (pages referred to as "RBr__") for a statement of Appellant's arguments thereagainst.

OPINION

Enablement

[2] It is not known why the Examiner chose to rely on § 102(b). It is not clear to us what subsection of § 102 the APA falls under. What is clear is that Appellant has admitted that figure 3 is prior art of some type. See In re Garfinkel, 437 F.2d 1000, 1004 n.2, 168 USPQ 659, 662 n.2 (CCPA 1971).

"The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation." United States v. Telectronics, Inc., 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988) (citing Hybritech, Inc. v. Monoclonal Antibodies, Inc., 802 F.2d 1367, 1384, 231 USPQ 81, 94 (Fed. Cir. 1986)). A patent need not teach, and preferably omits, what is well known in the art. Paperless Accounting, Inc. v. Bay Area Rapid Transit System, 804 F.2d 659, 664, 231 USPQ 649, 652 (Fed. Cir. 1986). The U.S. Patent and Trademark Office must support a rejection for lack of enablement with reasons. In re Marzocchi, 439 F.2d 220, 223-24, 169 USPQ 367, 369-70 (CCPA 1971).

The Examiner's position is as follows (EA5):

> The specification fails to enable how the circuit can use a "switching means formed in a semiconductor device having a p-type substrate with n-type wells", as recited in the claims. As discussed above, page 4 [sic, 3] [of the specification] makes it clear that the prior art circuit of Fig. 3 has a problem operating when switch S8 is an "n-channel transistor", which the specification somehow relates [to] a structure "formed in a semiconductor device having a p-type substrate with n-type wells". It is clear that switch S11 of the claimed invention shown in Fig. 4 similarly cannot be an "n-channel transistor". With this structure, it is clear

> that the circuit of Fig. 4 still will not provide a full range of operation. This is because S11 of Fig. 4 would still have the same problems disclosed with respect to the parasitic diodes when using an "n-channel transistor" for S8 of Fig. 3.

While the Examiner's rationale is not totally clear to us, we do our best to address it.

It is the claimed subject matter that must be enabled. Thus, it is the Examiner's duty to point out what language in the claim is not enabled. The language quoted by the Examiner in the first sentence is only found in canceled claim 1, not the claims on appeal. As best we can determine, the Examiner has a problem with the n-channel and p-channel limitations in the "wherein" clause of claim 8 and in claim 23, which is why claim 21 is not included in the rejection.

Before getting to the merits, the Examiner seems to have an objection to the terminology of "n-channel" and "p-substrate using an N-well process" at page 3 of the specification and also in the claims (EA6): "This disclosure is confusing because an 'n-type transistor' is not generally formed from 'p-type substrate having n-type well'". We do not see the problem. Appellant discloses a conventional N-well CMOS formation in figure 2, which has "a p-type substrate

having an n-type isolated well" (specification, p. 2, lines 7-8). A p-channel transistor is formed in the N-well and an n-channel transistor formed in the p-substrate (specification, p. 2, lines 8-10). Appellant discloses using both n-channel and p-channel transistors of this conventional CMOS formation shown in figure 2, having "a p-type substrate having an n-type isolated well" (specification, p. 2, lines 7-8); e.g., "in Figure 1, the voltage doubler requires one p-channel switch transistor S4 and three n-channel switch transistors S1, S2 and S3" (specification, p. 2, lines 24-26). Although there are other n-channel and p-channel structures, the transistors in the "wherein" clause of claim 8 and in claim 23 refer to the p-type substrate N-well CMOS structure of figure 2.

The specification does not disclose, and claims 8 and 23 do not recite, which transistors are n-channel and which are p-channel. However, the Examiner does not contend that the claims lack an enabling disclosure because one of ordinary skill in the art would not have had the skill to determine which switches should be made from n-channel transistors and which should be made from p-channel transistors. Instead, the

thrust of the non-enablement rejection appears to be that the circuit of figure 4 cannot be made to work with a full range of operation because if switch S11 were an "n-channel transistor," it would have the same problems with respect to parasitic diodes as disclosed when using an n-channel transistor for S8 in figure 3.

Appellant does not respond to this rationale. Nevertheless, we do not find the Examiner's reasoning persuasive. The Examiner concludes, without analysis, that switch S11 in figure 4 would have the same problem as switch S8 in figure 3 if it were made using an n-channel transistor. The specification discusses the problem with S8 as follows (p. 3, lines 23-28, as amended):

> [I]f switch S8 was made from an n-channel transistor 23 as shown in Figure 2, the N+ drain region 24 would be connected to a negative voltage V_{out}, while the substrate was connected to a higher voltage V_{ss}. The parasitic diode 28b of the transistor will be forward biased, and the output voltage V_{out} will be clamped to a maximum of one diode voltage drop below V_{ss}. [Emphasis added.]

This situation does not apply to S11 in figure 4 because one of the N+ regions would be connected to a positive voltage $2*V_{dd}$ during the second cycle. Thus, the parasitic diode will be reverse biased and will not have the problem of switch S8.

The Examiner has failed to establish a prima facie case of lack of enablement. The rejection of claims 8-10 and 23 is reversed.

Anticipation

Claims 8-10

Appellant argues that claim 8 recites "wherein said voltage generator is fabricated using p-channel enhancement mode transistors formed in n-type wells in a grounded p-type substrate and n-channel enhancement mode transistors formed in said grounded p-type substrate" and these limitations are not taught or suggested in figure 3 or the disclosure associated with figure 3 (Br9; RBr3). It is argued that figure 3 and its associated disclosure specifically points out why the negative voltage generator of figure 3 cannot be fabricated in this manner (Br9).

The Examiner's position is explained for the first time in the examiner's answer. The Examiner finds from the description of figure 3 that "[t]he conventional negative voltage generator is not preferably formed in a p-substrate using an N-well process because of the aforementioned parasitic diodes" (emphasis added) (specification, p. 3, lines 21-23) and that "the negative voltage generator is conventionally implemented with a P-well CMOS process" (emphasis added) (specification, p. 3, lines 28-30), that "one

skilled in the art would interpret this to state (i.e., anticipate) that the circuit of Fig. 3 can be such a structure [p-substrate with n-wells], while, it is preferred that [it] is not" (EA8). The Examiner finds that "even if S8 is an 'n-channel' as stated in line 24 of page 3 [of specification], it is clear that the circuit will still operate" (EA8).

Unfortunately, Appellant's reply brief does not address these reasons. The Examiner's finding that the description of figure 3 teaches that it is possible, just not preferable or conventional, to implement the conventional negative voltage generator in a p-substrate with an n-well CMOS process instead of with a p-well CMOS process seems reasonable. We are not inclined to reverse the Examiner's finding absent some argument by Appellant why the Examiner errs or why the specification should be interpreted in another way. Appellant has also not responded to the Examiner's finding that the circuit would work if S8 was an n-channel transistor in a grounded p-substrate. The specification states that it is an "object to provide a negative voltage generator using N-well CMOS technology which can generate a voltage more negative than a parasitic diode voltage drop" (specification, p. 4,

lines 1-3), which implies that a voltage more negative than a parasitic diode voltage drop (discussed as the problem with an n-channel N-well implementation) is desired, but not required. Because Appellant has not shown error in the Examiner's findings, we sustain the rejection of claims 8-10.

Claims 21 and 23

In claim 21: (1) there is no antecedent basis for the first occurrence of "said supply voltage"; and (2) it is unclear where the "output voltage" is produced.

Appellant argues that claim 21 recites "a voltage enhancement circuit connected to said supply voltage that generates an enhanced voltage that is greater than said supply voltage," "a capacitor having a first node connected to said enhanced voltage and a second node connected to said supply voltage during a first phase," and "switches that disconnect said first and second nodes of said capacitor from said supply voltage and connect said first node to a reference voltage, that is less than said supply voltage, during a second phase to produce an output voltage that is less than said reference voltage during said second phase," none of which are remotely taught or suggested in figure 3 or the disclosure associated with figure 3 (Br9; RBr3). It is argued that figure 3 does not teach using an enhanced voltage or connecting a capacitor between an enhanced voltage and a supply voltage (Br10).

We agree that these limitations of claim 21 are not disclosed in figure 3 or the accompanying discussion. The

Examiner does not even attempt to address these limitations in the final rejection or the examiner's answer. Accordingly, the anticipation rejection of claims 21 and 23 is reversed.

CONCLUSION

The rejection of claims 8-10 and 23 under 35 U.S.C. § 112, first paragraph, lack of enablement is reversed.

The rejection of claims 8-10 under § 102 is sustained.

The rejection of claims 21 and 23 under § 102 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

ERROL A. KRASS)
Administrative Patent Judge)
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) BOARD OF PATENT

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